Abstract

[0033] An improved method and circuit for reduced settling time in an amplifier are provided. The amplifier comprises a composite amplifier circuit including a first amplifier configured with a second amplifier comprising an integrator circuit. The reduced settling time is facilitated through implementation of a faster path configured between an inverting input terminal of the second amplifier and an output terminal of the first amplifier for current needed by an integrator resistor due to any signal appearing at said inverting input terminal for said high-speed amplifier. The faster path can be realized through the addition of a compensation capacitor between the output terminal of the composite amplifier circuit and the inverting input terminal of the second amplifier. The compensation capacitor can comprise various values depending on any given number of design criteria. The additional path can also minimize the settling time effects from process variations in the various resistors and capacitors, as well as the amplifier gains, realized in the composite amplifier circuit.